DoGav Systems

COALESCING FOR THE POWERQUICC II

Data Sheet
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Part Number: DG02010901

PRODUCT DESCRIPTION

Coalescing is a feature of the PowerQUICC II Pro and PowerQUICC III families aimed at minimizing the overhead associated with interrupt handling.

When a driver is designed to handle receive (Rx) or transmit (Tx) events as soon as they occur in order to match real-time requirements, it may severely affect the overall system performance, particularly in a heavy traffic environment. This is due to the overhead associated with the frequent accessing and exiting the interrupt handler. This context switching is particularly costly because of the requirement to always save and restore the content of the GPRs (General Purpose Register) and some of the SPRs (Special Purpose Register) whenever an interrupt is triggered.

This coalescing microcode module offers similar functionality for the PowerQUICC II family. It enables the system to continue to maintain real-time performance, whilst reducing the cost of the context switching by sharing the overhead associated with interrupts between a configurable number of events. The user can control the parameter which dictates after how many events (e.g. received frames) an interrupt is generated.

The module also deals with aging events. These are pending events waiting for the pre-defined number of pending event threshold to be satisfied in order for an interrupt to be triggered. In addition to the threshold parameter the user can also set a time-out parameter which triggers an interrupt even when the threshold is not reached.

A simple diagram illustrating the operation of the module can be found below.

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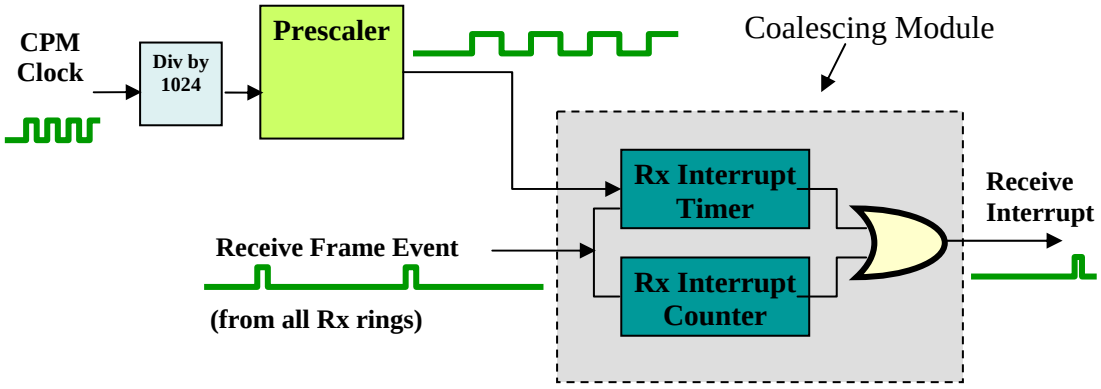

- Interrupt counters reduce number of interrupts triggered to one per *N* frames.
- Timers ensure that interrupts occur even under little or no network activity.

MAIN FEATURES

- Implemented for PowerQUICC II FCC Ethernet receiver
- Dramatically reduces the host Interrupt overhead
- Configurable threshold
- Configurable time-out
- Parameters can be dynamically updated by the user application
- 32-bit statistical counters:
    - Number of interrupts generated as a result of threshold value reached
    - Number of interrupts generated as a result of time-out expiration
    - Number of times events occurred (e.g. frame received).
    - Number of times the time-out timer expired (interrupts were not necessarily generated).
- Very small footprint (negligible impact on the CPM activities)
- Maintains a 24-bytes data structure per FCC that contains all the parameters and statistical counters
- Easily integrated into existing user applications. No code modification is required, except some additional initialization code
- Supports all PowerQUICC II versions

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Note:
The module can be further customized to meet specific requirements. For more details please contact DoGav Systems.

MICROCODE TRAP USAGE

The coalescing module consumes two CPM traps out of the four (or eight) traps available.

ABOUT DOGAV SYSTEMS

DoGav Systems is a leading provider of software and hardware consultancy and training services. It specializes in Freescale's processors, in particular the PowerQUICC family of communication processors. It has a proven track record of over 20 years supporting Freescale customers in developing market-leading products for the communications equipment market.

DoGav Systems is Freescale's most experienced and active microcode developer. Since receiving its license in 2000, it has developed numerous customized microcode packages for both small and large Freescale customers. These packages are now successfully deployed in commercial products. In addition, DoGav Systems also offers more than 30 off-the-shelf microcode products for the PowerQUICC I, PowerQUICC II, PowerQUICC III and PowerQUICC II Pro processors.

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