DOGAV SYSTEMS LTD.

MemTest (microcode version)

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1. Acronyms

Abbr.	Description	Comment
char	Character	
CPM	Communication Processor module	MPC82xx devices
DPR	Dual-Ported RAM	MPC82xx devices
EUU	Exclusive Microcode Usage	
FSL	Freescale	
IRAM	CPM/QE Instruction RAM	
ITZ	Initialize to Zero	
MBA	Must be Aligned	
MURAM	Multi User Ram	MPC83xx and MPC85xx devices
NA	Not Applicable	
QE	FSL's QUICC Engine	MPC83xx and MPC85xx devices
Ucode	QE RISC Microcode	
uSec	Micro Second	

2. References

- MPC8360E PowerQUICC™ II Pro Integrated Communications Processor Family Reference Manual (rev. Rev. 2 05/2007)
- QEIWRM QUICC Engine™ Block Reference Manual with Protocol Interworking (Rev. 3.0)

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3. Introduction

MemTest is a memory testing tool for systems designed with Freescale's CPM-based and QUICC Engine (QE)-based PowerQUICC devices. The tool is implemented in microcode and runs on the CPM or the QE. It can be used with Static, Dynamic, SDRAM, or DDRx, and works by flooding the memory under test with well distributed pseudo random data, and then verifies the integrity of this data.

The MemTest microcode module is much more than just a memory testing tool. It can also be used with the increasingly popular DDRx memory to both adjust and fine-tune its sensitive timing. Because of the module's very small footprint it can be downloaded into the internal DPRAM by the COP/BDM port, and still leave enough free space on the DPRAM to include extensive error reporting if required.

The following features are supported:

- Simulates very heavy/stressed bus activity during memory testing
- Helps to configure the DDR(s) memory timing even before Flash
- 32-bit preset value enables 4,294,967,295(!) different pseudo random pattern sequences
- Quits after a specified number of detected errors
- Provides comprehensive reporting: Bad-address, Read-data, Expected-data, XOR (helps to detect possible cross-talk or bad lane)
- Extremely fast (on a MPC830E MDS board, QE=400MHz and CCB/DDR= 266MHz, the module is able to test DDR1's 32MByte of memory in less than 680 MSec!)
- Not affected by data core-cache. CPM/QE uses its internal DMA to generate memory write/read transactions.
- Can optionally perform random reads from a configurable address range during the memory fill, to mix different bus operations (this option available on request and charged separately)
- Application can perform FILL only, CHECK only, FILL-and-CHECK (typically used) and FILL-and-CHECK-and-Prepare-for-Next-Test (set new preset)
- Provides testing time with a configurable resolution
- Generates event (interrupt) upon test completion

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4. Product Description

DoGav's Systems MemTest microcode version is available for CPM and QE communication RISCs. The RISC API is identical for both implementations.

The ucode image must be uploaded as a patch, into the CPM/QE IRAM. DoGav Systems provides a C-function that installs the ucode. See section 10 for details.

The test is invoked by a CPM/QE command. Before the test command is invoked, test parameters must be initialized. Some examples of test parameters that need to be initialized are: memory start address, size of memory to be tested (in bytes), where to record mismatch errors, etc.

The test is destructive! All memory-tested area is lost. Therefore, the application should not provide test-memory that contains code, heaps, stacks, etc.

Caution must be taken for MMU-based environments. All provided addresses must be **physical** values!

5. Data structures

The application must allocate a 128-byte data structure to hold input test parameters, ucode temporary variables, test status and results. Additionally, an error report table must be allocated. The size of the table is dictated by the number of report errors the application asks for. Each error corresponds to 16-byte entry. Both the MemTest structure and the error table must reside on MURAM/DPR. Some of the parameters are subject to alignment restriction.

Table 1 below depicts the MemTest structure details

Table 1: MemTest Structure

OFFSET (HEX)	**Name**	**Size** (bytes)	**Description**
00	Result	2	Reports test result. See details below.
02	Rsrv_o2	4	Reserved, ITZ
04	**Start_Addr**	4	Memory starts address. Must be aligned to 32!
08	**size_byte**	4	Number of bytes to be tested starting from Start_Addr. Must be aligned to 32!
0C	**Test_num**	4	Test Number. There are about 4G different tests. This provided value determines the preset value for pseudo random data generation.

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10	check_time	4	Test duration. If the CPM/QE timestamp timer is enabled (with an application-selected prescale) the ucode will provide the test time in check_time. See details below.
14	euu_14	4	EUU. ITZ.
18	**error_addr**	2	CPM/QE DPR/MURAM address of the error report table. Each entry in the table occupies 16 bytes. See details below.
1A	**num_of_error**	2	Number of errors to be reported. If CHECK process reaches this number, the test stops. See details below. Must be at least 1!
1C	euu_1C	4	EUU
20	**Read_Inj_start**	4	ITZ (must!)
24	**Read_Inj_mask**	4	ITZ
28	euu_28	4	EUU
2C	date	3	Ucode current version date in format: dd:mm:yy
2F	uc_ver	1	Ucode version/revision. Hex values are used.
30	reserved	2	ITZ
32	euu_32	4	EUU
34	**RD_Buff_addr**	2	Address of read_buff
36	**WR_Buff_addr**	2	Address of write_buffer
38	euu_38	4	EUU
3c	**Test Type**	2	Request test type. See details below
40	write_buffer	32	EUU
60	read buff	32	EUU

EUU = Exclusive Ucode Usage.

ITZ= Init To Zero.

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6. Parameters Details

This section details selected parameters of the MemTest data structure as define in Table 1 above.

Result The test result is reported here. While the test is being carried out, the value in Result is 0x**E**FFF or 0x**E**CCC. When the test is completed, Result will contain the Number of Errors (mismatch) found. 0 indicates that the test passed and no error was found.

If test type is unknown (as provided in the test type parameter), Result will display the value: 0x**0**EEE.

The application must wait for the test to be completed. This is achieved by sampling Result for a value other than 0xECEC_0000.

Test_num This value determines the test number. There are about 4G different tests. This value is used as the first preset to the pseudo random generator.

A zero value is not allowed. In this case the value is set internally by the ucode to 0x1234.

The application may select a test that automatically increments this value, as a preparation for the next test. This mode is useful when multiple tests are required (typically overnight or on the weekend, right after board assembly).

check_time If the CPM/QE time-stamp timer is enabled, the ucode will provide the test time (time-stamp ticks) in check_time.

For CPM, the **RTSCR** register (offset 0x119DC) must be initialized with the desired prescale.

For QE, the **CETSCR** register (offset 0x0011C) must be initialized with the desired prescale. Time-stamp2 is used (RTE2 and CETPS2 should be configured).

error_addr The application must allocate space for an error table. This table must reside on DPR/MURAM and is used for error (mismatch) reporting. The size of the table depends on number of errors the application permits before it stops the test. Each error occupies a 16-byte entry. See section 7 for the error entry format.

Because the table resides on DPR/MURAM memory, only a two-byte pointer (offset) is required.

num_of_error Number of reported errors (if any) allowed before the test stops.

Must be at least 1.

RD_Buff_addr Least Significant 16 bit of the absolute address of read_buff.

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WR_Buff_addr Least Significant 16 bit of the absolute address of write_buff.

Test_type The type of memory test to run. Refer to section 9 below for details on the different types of memory tests.

7. Error Table Format

The error table must be located on the DPR/MURAM internal memory. Its start address must be aligned to 16.

After the FILL phase of the test, the CHECK phase may begin, where the test memory is read (either 4 bytes at a time or in a burst of 32 bytes) and compared with the expected content. If a mismatch is detected, it is reported on the error table. Each mismatch occupies an error entry.

Each entry contains four 4-byte elements (a total of 16 bytes per entry) as detailed in Table 2 below.

Table 2: Error Entry Format

OFFSET (HEX)	**Name**	**Size** (bytes)	**Description**
0	Error Address	4	Tested memory address where an error is detected
4	Expected Data	4	What data (4 bytes) were written to memory
8	Actual Data	4	What data was read from memory (either as a single word or a burst)
C	XOR	4	Exclusive OR between write and read data

The XOR helps to detect cross talk between two (or more) wires, or, in the case of DDR memory, incorrect strobe byte timing.

Note:

Application must set MemTest's parameter num_of_error to report at least one mismatch error!

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8. DPR/MURAM usage

The internal memory usage is minimal. Only the data structure and the error table must be allocated. See Table 3 below for details.

Table 3: MemTest Internal Memory requirements

Category	Size Hex (dec)	Required Alignment	Comment
Data structure	0x80 (128)	256 †	
Error Table	0x100 (256)	16	If test is configured for 16 error report
Total	**0x180 (384)**		

† If CPM is used, because SCC requirements

9. Tests types

MemTest supports 3 test types.

The test consists of two phases:

- FILL: The tested memory is filled with pseudo random data (either 4 bytes or 32bytes at a time)
- CHECK: The tested memory is read and compared with the expected filled data

Normally the test runs sequentially: the CHECK phase follows the FILL phase automatically. However, the application may request to separate the FILL phase from the CHECK phase and instruct the test to stop after the FILL, or to perform the CHECK phase only. This CHECK phase only feature may be used by a customer to "gain" confidence at the test: the customer manually modifies a selected area of memory, and then runs the CHECK phase to see if the data that was manually written is detected.

Some customers would like to run extended tests overnight or on the weekend. MemTest allows the application to automatically run test after test. To do this, test_type 4 or 12 must be selected (test_type 4 for burst cycles and test_type 12 for single 4-byte cycles). When test_type 4 or 12 is selected, Test_num is internally incremented upon completion of the current test, in preparation for the next test. The application must then invoke the start test command again. See 11 on page 13 for details. Note that the command value depends on the platform device (CPM or QE).

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Table 4: Supported MemTest types

Station Type	Code (dec)	Description	Bus Cycle Mode
FILL Only	1	Fill tested memory with pseudo random data and stop	Burst
CHECK Only	2	Check tested memory for data mismatch	Burst
FILL followed by CHECK	3	Perform CHECK immediately after FILL and stop	Burst
FILL followed by CHECK and prepare for next test	4	Perform CHECK immediately after FILL. Upon completion, increment test number and stop.	Burst
FILL Only	9	Fill tested memory with pseudo random data and stop	Single (4-byte at a time)
CHECK Only	10	Check tested memory for data mismatch	Single (4-byte at a time)
FILL followed by CHECK	11	Perform CHECK immediately after FILL and stop	Single (4-byte at a time)
FILL followed by CHECK and prepare for next test	12	Perform CHECK immediately after FILL. Upon completion, increment test number and stop.	Single (4-byte at a time)

Note:

QE devices are typically connected to DDR. Therefore Read/Write transactions are dictated by the memory controller as burst only. A single write is implemented as read-modify-write.

CPM devices are implemented with SDRAM; therefore, the test offers both single (4 bytes at the time) and burst (32 bytes at a time) bus cycle options.

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10. Microcode Installation

DoGav Systems provides a ucode package that includes:

- Ucode image (h-file)
- C-function that installs the ucode and associated h-files
- H-files where the various MemTest structures are defined

The c-function checks the actual silicon version and selects the right image. Then the selected image is installed into the QE I-RAM via QE registers IADD and IDATA. The function also sets up the corresponding traps registers.

Note:

DoGav Systems must be notified in advanced if the application uses other ucode patches on the same platform. These patches must be integrated with the MemTest ucode into a single module.

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11. Specific Implementation

This section describes the implementation of the specific device. Because of the different nature of the CPM and QE, this section is divided into two sub sections: one for CPM and one for QE.

11.1. CPM Implementation

In the CPM implementation, MemTest uses one of the four SCCs. The actual SCC is determined by the specific application. A typical application doesn't implement all four SCCs, so normally Mem_Test does not get in the way of testing an application. Even if an application does use all four SCCs, MemTest is minimally disruptive, since it is normally used only during the early phase of board qualification or as BIT right after boot. This way the "lost SCC" may be recovered. This also implies that the MemTest structure should be placed as specified in Table 5 below.

Table 5: CPM data structure location

SCC	Location (offset from IMMR)	CPCR Command
SCC1	0x8000	0x0081_001F
SCC2	0x8100	0x04A1_001F
SCC3	0x8200	0x08C1_001F
SCC4	0x8300	0x0CE1_001F

In order to invoke the test, a CPM command must be issued. The command should be issued only after all parameters are provided. Table 5 specifies the command value, per SCC, that should be issued to the register CPCR.

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11.2. QE Implementation

Due to QE's programming model flexibility, the application may allocate the MemTest data structure anywhere on the MURAM, subject to 64 (0x40) alignment restrictions. However, (0x80) alignment is recommended.

Two setup commands must be issued to register CECR (and CECDR in some cases) as described in Table 6. SNUM 0xF8 must be used.

Table 6: QE Commands

Command	CECR	CECDR	Description
Assign Page	0x01F1_0012	MemTest Data Structure address (only LS-16 bits)	Informs QE where Data Structure is located
Use Single QE RISC	0x01F1_0110	NA	Instructs the QE to RUN only RISC1 for MemTest†
Run MemTest	0x01F1_0060	NA	Invokes MemTest. Selected type will be executed ††

† Relevant only for multi-RISC QE (e.g. MPC8568). This command has no effect for a single RISC QE device.

†† See section 9 for test types details.

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12. Test Completion

When the test is running, the Result's MS-nibble is set to hex 0xE (signifying Execution in Process). When the test is completed, the MS-nibble is cleared. This MS-nibble can be polled by the application to detect test completion. The application may prefer to poll an event (i.e. expect an interrupt) instead. See section 13 for details. Table 7 below summarizes Result's possible values.

Table 7: Possible Result values

Test state	Result Display	Comment
FILL	0x**E**FFF	In FILL Phase
CHECK	0x**E**CCC	In CHECK Phase
FILL Only Completion	0x**0**000	FILL Phase Complete
CHECK Completion	Number of mismatches found	CHECK Phase Complete
Wrong Input Parameter	0x**0**EEE	Indicates Test_type = 0 (invalid parameter)

13. MemTest Events

MemTest generates a completion event when the test finishes either successfully or with one or more error. In addition, if a mismatch is detected during the CHECK phase, another event is set as described by Table 8.

Table 8: Events generated by MemTest

Event	Value	Comment
MemTest completion	0x80	
Error	0x40	Actual value 0xC0 to signify completion with error

If the CPM device is used, the event register is $SCCE_x$ and the mask register is $SCCM_x$ where x depends on which SCC number (one of four) is assigned for MemTest.
If the QE device is used, the event register is CEEXE1 (offset QE-base + 0x160) and the mask register is CEEXM1 (offset QE-base + 0x164).
If the event is not masked, an interrupt will be generated.

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14. MemTest Examples (Captured Snapshots)

This section shows some snapshots of memory before and after MemTest. The following snapshots are captured for the CPM device test (MPC8280) with the following set-up parameters:

Table 9: Parameters used by MemTest snapshot

Parameter	Address	Comments
MemTest_t	0x047_8000	MemTest structure
Start_Addr	0x0010_0000	Tested memory start address (1M)
size_byte	0x00F0_0000	Tested memory size (15M)
Test_num	0x0000_0001	Test number
error_addr	0x8080	Location (on MURAM) of error-report table
num_of_error	0x10	Request to quit after 16 errors
Read_Inj_start	0	(not used)
Read_Inj_mask	0	(not used)
Test_Type	1	Test type: FILL only
RD_Buff_addr	0x8060	Pointers to burst read buffer (CPM only)
WR_Buff_addr	0x8040	Pointers to burst write buffer (CPM only)

Figure 1 below shows the MemTest structure and the section of the tested memory before the test is invoked. In Figure 1, the memory labelled Memory 1 and Memory 2 shows the MemTest structure; the memory labelled Memory 3 shows the start of the test memory area; and the memory labelled Memory 4 shows the end of the test memory area. The tested memory is filled by the c-function (memset) with 0x99.

Figure 2 shows the memory content after FILL. As expected the filled data is “random”.

Error! Reference source not found. shows the memory after it was manually modified. Four locations have been modified:

1. 0x010_0000 (filled with `0xAAAA_AAAA`)
2. 0x010_0044 (filled with `0xBBBB_BBBB`)
3. 0xFF_FFC8 (filled with `0xCCCC_CCCC`)
4. 0xFF_FFFC (filled with `0xDDDD_DDDD`)

Figure 4 shows the MemTest result after running CHECK (Test_Type = 2). As expected all four mismatches were detected and reported in the error table. In addition, MemTest set the Result parameter to 4.

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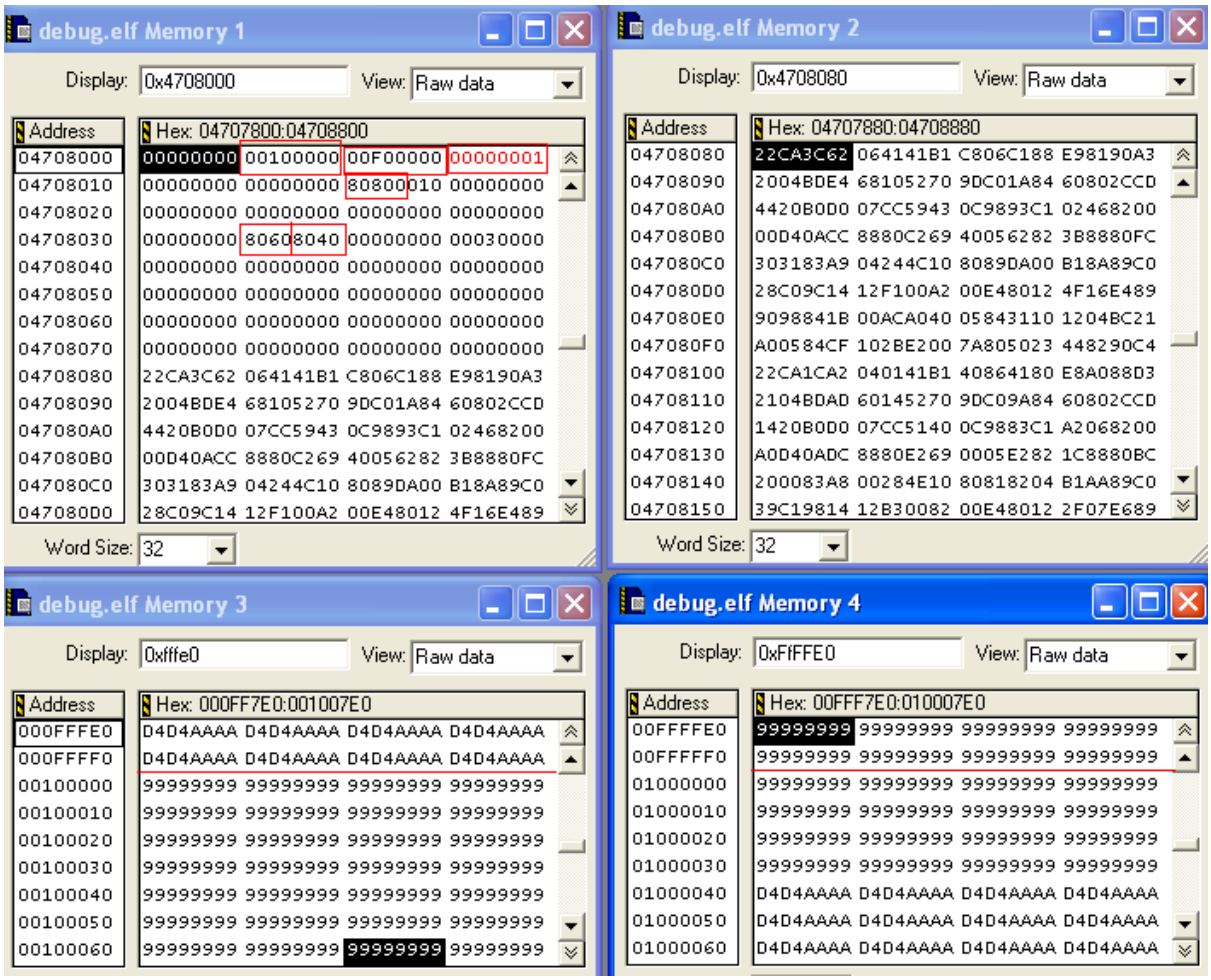

Figure 1: MemTest structure and tested memory before test begins

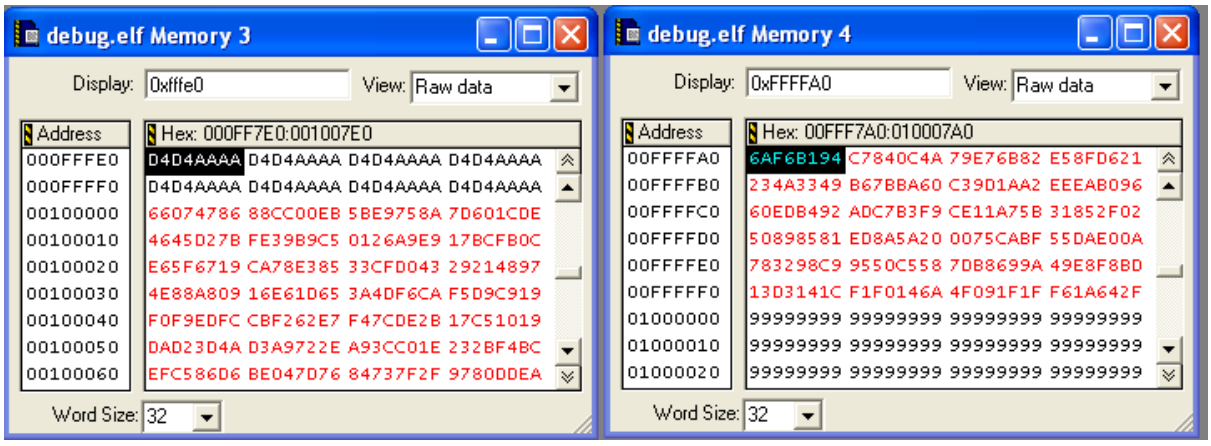

Figure 2: Memory after FILL

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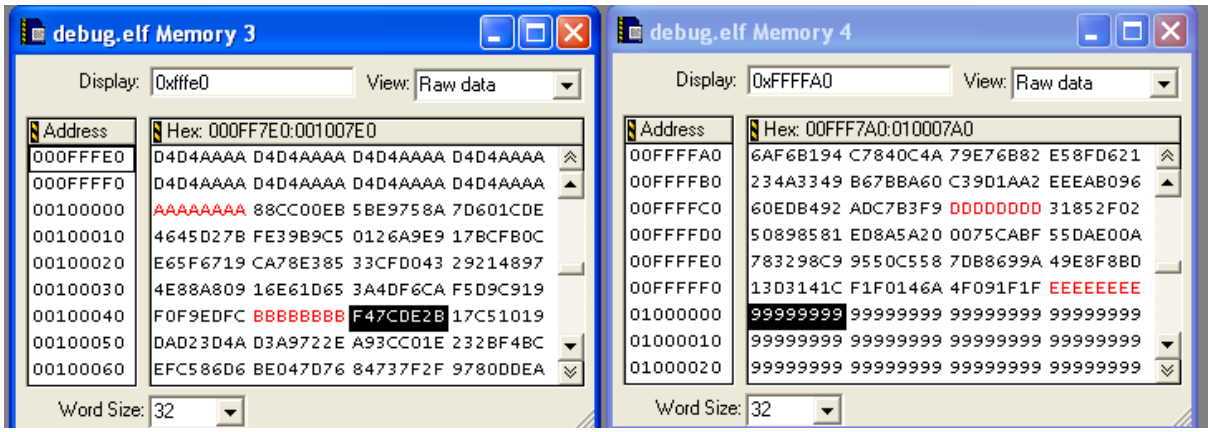

Figure 3: Memory after manual modification

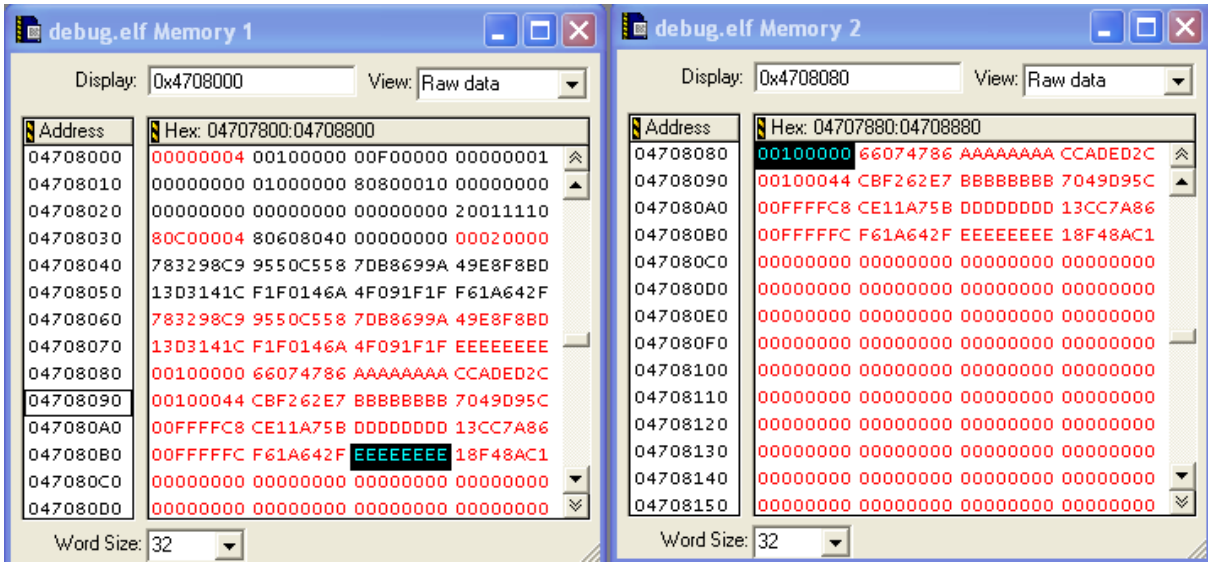

Figure 4: Error Table after CHECK

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ABOUT DOGAV SYSTEMS

DoGav Systems is a leading provider of software and hardware consultancy and training services. It specializes in Freescale's processors, in particular the PowerQUICC family of communication processors. It has a proven track record of over 25 years supporting Freescale (Motorola) customers in developing market-leading products for the communications equipment market.

DoGav Systems is Freescale's most experienced and active microcode developer. Since receiving its license in 2000, it has developed numerous customized microcode packages for both small and large Freescale customers. These packages are now successfully deployed in commercial products. In addition, DoGav Systems also offers more than 30 off-the-shelf microcode products for the PowerQUICC I, PowerQUICC II, PowerQUICC III, PowerQUICC II Pro, PowerQUICC III and QorIQ processors

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