

IP Filter Microcode Module

Data Sheet
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PRODUCT DESCRIPTION

The IP Filter microcode module is used to filter Ethernet frames based on an exact match of IP addresses. The matched frames are routed to up to eight (typically seven) receive BD rings, based on the filtered IP address. The eighth ring can be used either for “none-matching” frames, or as an additional IP matched ring.

The user can append and/or cancel IP addresses to be matched dynamically. The “search for match” algorithm incorporates an efficient hashing algorithm. The primary hash table is stored on the internal DPRAM, and therefore the number of IP addresses that can be matched is heavily dependant on the amount of available DPRAM space. Tests in a real life environment showed that, on average, up to 4K of IP addresses can be supported efficiently. The module permits up to 32K IP addresses.

Main features include:

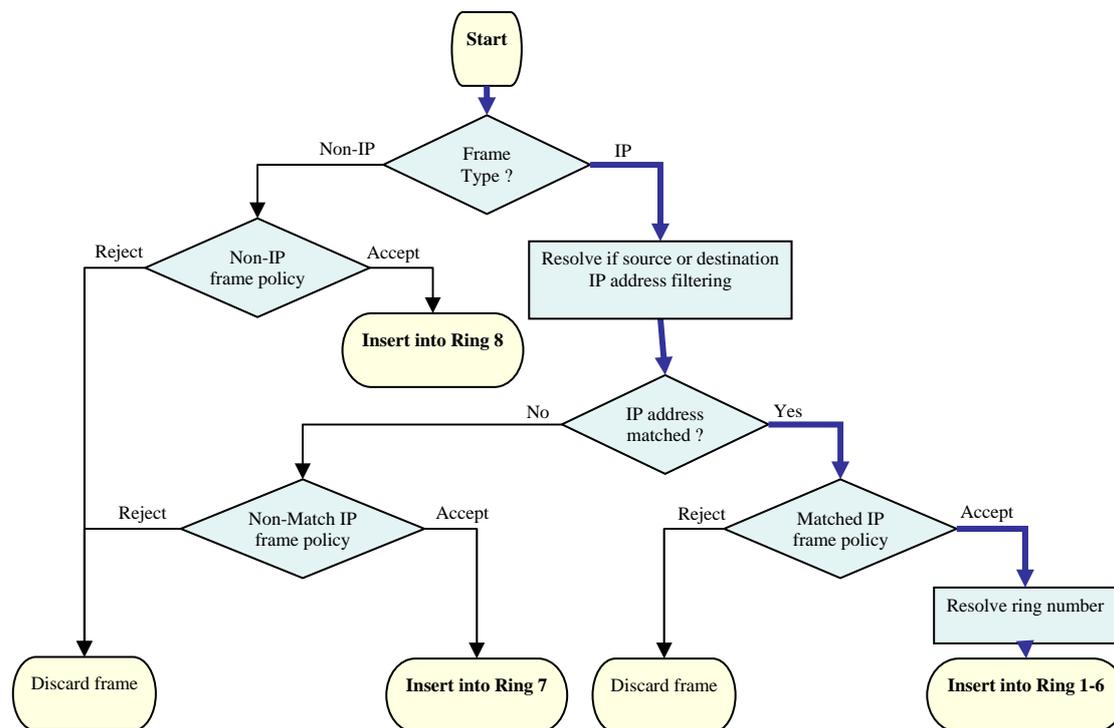
- IP address filtering based on exact match
- Either source IP or destination IP address of the incoming frame is compared (globally selected)
- Supports up to 2K IP addresses, with the option to customize the number of IP addresses at the expense of DPRAM space
- List of IP addresses to be matched can be dynamically modified
- Addresses are stored on an external memory (either 60x or local bus)
- Supports IP address range by associating a user-supplied mask with each IP address.
- Recognizes and supports IP header encapsulated inside VLAN
- Search algorithm incorporates efficient multi level hash tables, with primary hash table resides on DPRAM
- Can optionally verify the IP header checksum and discard incorrect frame
- Global policy of non-IP frame (Accept/Discard) is selectable. If Accept is selected, non-IP frames (e.g. ARP) are tagged with a bit in the RxBD.
- Three statistics 32-bit counters: number of IP-hit frames, number of IP-miss frames, number of non-IP frames
- Supports filtering of a range of IP addresses at a cost of a single entry in the look up table



The key benefits of the module are:

- Saves significantly on Host processing time
- Reduces bus activity (discarded frames are not stored in memory)
- Enables the application to set up different priorities to different IP address

A flow chart illustrating the operation of the module is presented below.



Note:

The module can be further customized to meet specific requirements such as, for example, filtering based on port number (in case of UDP frame), etc. For more details please contact DoGav Systems.

MICROCODE TRAP USAGE

The module uses 3 traps.

MICROCODE VERSION

This microcode module is mask version dependent, and a facility is provided to select the proper version dependent module.

Notes:

In older PQII revisions (HIP 3) the microcode module is installed in the “user DPRAM” portion. If the user intends to use this module with these versions, 2K bytes at the beginning of the DPRAM are not available for the application. Refer to the PQII user manual sub-section “Dual-Port RAM” of the Communications Processor Module Overview chapter.

ABOUT DOGAV SYSTEMS

DoGav Systems is a leading provider of software and hardware consultancy and training services. It specializes in Freescale's processors, in particular the PowerQUICC family of communication processors. It has a proven track record of over 20 years supporting Freescale customers in developing market-leading products for the communications equipment market.

DoGav Systems is Freescale's most experienced and active microcode developer. Since receiving its license in 2000, it has developed numerous customized microcode packages for both small and large Freescale customers. These packages are now successfully deployed in commercial products. In addition, DoGav Systems also offers more than 30 off-the-shelf microcode products for the PowerQUICC I, PowerQUICC II, PowerQUICC III and PowerQUICC II Pro processors.

